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10/791,175	03/02/2004	Hayden C. Cranford JR.	RPS920030105US1/2872P	3190

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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
04/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/791,175	CRANFORD ET AL.	
	Examiner	Art Unit	
	SIU M. LEE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 12 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 12 and 18 recites the limitation "the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals". According to figure 2 of the instant application, the adder is accumulating the chosen most significant bit of the up/down counter instead of the chosen most significant bits of the rotate up and rotate down signals.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-11, 13-17, 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii (US 5,349,309).

(1) Regarding claim 1:

Fujii discloses a circuit comprising:

a controller (phase frequency detector (pfd) 2 in figure 2) for generating first rotate up and rotate down signals (the examiner interpret the LEAD, LAG signal output by phase frequency detector 2 as the rotate up and rotate down signal) for phase adjusts in a receiver link to adapt to frequency offsets (phase frequency detector 2 for comparing the output of the oscillating circuit 7 and a signal IN given to an input terminal 1 to emit a signal LEAD or LAG according to the phase difference, column 3, line68 – column 4, line 3), the first rotate up and rotate down signals (the examiner interpret the LEAD, LAG signal output by phase frequency detector 2 as the rotate up and rotate down signal) causing rotation of a phase of a clock signal up or down to compensate for the frequency offsets (the LEAD, LAG signal from PFD 2 is forward to register 5 and then to adder 6 and the output of adder 6 will control the oscillator 7 according to the output of adder 6, column 54, lines 17-26, 55-62) ; and

an adjust circuit (random walk filter (RWF) 3 and up down counter 4 in figure 2) coupled to the controller (RWF 3 is connected to the PFD 2 as shown in figure 2), the

adjust circuit for detecting trends in the first rotate up and rotate down signals (the RWF 3 reads the output of the phase/frequency detector 2 at a predetermined clock cycle. If the input at that time is LEAD, then the internal up-down counter operates by +1, if LAG, then by -1 and if neither of them, then by 0 respectively; if the count value of the up-down counter adds up to +N, then the UP is emitted to return to the initial value (0). On the other hand, if the count value of the up-down counter becomes -N, then the DOWN is emitted to return to the initial value, column 4, lines 27-40), and using combinatorial logic (adder 6 in figure 2) to adapt the first rotate up and rotate down signals for the phase adjusts based on accumulated data accumulated by an adder (the up down counter 4) (adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62) by generating second rotate up and rotate down signals (the output of the adder 6 in figure 2) improving a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets (the present invention object is to provide a phase locked loop in which the freedom of choice of the loop bandwidth is large and therefore a desire loop bandwidth can be obtained, column 6, lines 21-23; it is well known in the art that for a phase lock loop with a desire loop bandwidth will improve the system response and thus improve rate of compensation for the frequency offset).

(2) Regarding claim 3:

Fujii discloses that wherein the adjust circuit monitors for an overflow of the first rotate up and rotate down signals (if the count value of the up-down counter adds up to

+N, then the UP is emitted to return to the initial value (0). On the other hand, if the count value of the up-down counter becomes -N, then the DOWN is emitted to return to the initial value, column 4, lines 25-40).

(3) Regarding claim 4:

Fujii discloses wherein the adjust circuit monitors for an overflow by counting and accumulating the first rotate up and rotate down signals (if the count value of the up-down counter adds up to +N, then the UP is emitted to return to the initial value (0). On the other hand, if the count value of the up-down counter becomes -N, then the DOWN is emitted to return to the initial value, column 4, lines 25-40).

(4) Regarding claim 5:

Fujii discloses wherein the adjust circuit monitors for an overflow with an up/down counter coupled to the adder (the RWF 3 has an internal up down counter to monitor the LEAD and LAG signal from the PFD 2, column 4, lines 25-40).

(5) Regarding claim 6:

Fujii discloses wherein the adjust circuit generates the second rotate up and rotate down signals through detection of overflow and underflow in the adder (counter 4 with respect to figure 5, if the UP is entered from the random walk filter 3, the internal up-down counter operates by +1, if the DOWN is entered, then by -1, the UP and DOWN are sequentially calculated to accumulate the result; if the count value becomes +M (overflow), even if the UP is further entered, the count value is not changed; if the count value becomes –M (underflow), even if the DOWN is further entered, the count value is not changed any more; counter 4 emits this count value to the adder 6 as the n-

bit signal, column 4, lines 45-54) and logically combines by the combinatorial logic the overflow and underflow with the first rotate up and rotate down signals (adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(6) Regarding claim 7:

Fujii discloses a circuit comprising:

an up/down counter (internal up down counter in the random walk filter 3 in figure 2) for counting signals from a phase rotator control (phase frequency detector 2 in figure 2) for phase adjustments by a clock-data-recovery loop of a serial receiver (it is well known that a phase lock loop is used in a clock-data recovery loop of a serial receiver); and

an adder (counter 4 in figure 2) coupled to the up/down counter (internal up down counter of RWF 3) that outputs accumulated data indicative of a trend in the phase adjustments (the internal up down counter of RWF 3 accumulate the LEAD, LAG signal from the phase frequency detector 2) (the UP and DOWN signal from the RWF3 are sequentially calculated to accumulate the result by the counter 4, column 4, lines 45-49).

(7) Regarding claim 8:

Fujii discloses wherein the signals comprise rotate up and rotate down signals (the examiner interpret the LEAD, LAG signal from the phase frequency detector 2 as the rotate up and rotate down signals).

(8) Regarding claim 9:

Fujii discloses the circuit further comprising combinatorial logic (adder 6 in figure 2) coupled to the adder (counter 4) to adapt the rotate up and rotate down signals based on the accumulated data (adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(9) Regarding claim 10:

Fujii discloses wherein the combinatorial logic generates a new rotate up signal based on an overflow in the adder (for the counter 4, if the count value becomes +M (overflow), the counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54; the adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(10) Regarding claim 11:

Fujii discloses wherein the combinatorial logic generates a new rotate down signal based on an underflow in the adder (for the counter 4, if the count value becomes –M (underflow), the counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54; the adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(11) Regarding claim 13:

Fujii discloses a method comprising:

monitoring trends of phase adjusts of signals from a phase rotator control of a clock-data-recovery circuit to a reference clock of a serial receiver (phase/frequency detector 2 compare the output (REF) of the oscillating circuit 7 and a signal IN given to an input terminal 1 to emit a signal LEAD or LAG according to that phase difference; a

random walk filter 3 for emitting an up pulse (hereinafter referred to as UP) or a down pulse (hereinafter referred to as DOWN) according to the output of the phase/frequency detector 2, column 3, line 68 - column 4, line 7); and

adapting the phase adjusts to create future adjusts based on previous adjusts (the adder 6 adds the output of the counter 4 (output of counter 4 depends on the output of the RWF 3) and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(12) Regarding claim 14:

Fujii discloses wherein the step of monitoring further comprises utilizing an up-down counter (the RWF 3 has an internal up down counter, column 4, lines 31-35) and an adder (counter 4 in figure 2) to accumulate phase adjust data from the phase adjusts (the UP and DOWN signal from the RWF3 are sequentially calculated to accumulate the result by the counter 4, column 4, lines 45-49).

(13) Regarding claim 15:

Fujii discloses the method further comprising utilizing combinatorial logic (adder 6 in figure 2) to generate the future adjusts based on the accumulated phase adjust data and the previous adjusts (the adder 6 adds the output of the counter 4 (previous adjust) and the output of the register 5 (present adjust) to emit the result (future adjust) to the oscillator 7, column 4, lines 60-62).

(14) Regarding claim 16:

Fujii discloses wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data-recovery circuit (phase/frequency

detector 2 compare the output (REF) of the oscillating circuit 7 and a signal IN given to an input terminal 1 to emit a signal LEAD or LAG according to that phase difference, column 3, lines 68 - column 4, line 3) and wherein utilizing the combinatorial logic includes generating a new rotate up signal based on an overflow in the adder (for the counter 4, if the count value becomes +M (overflow), the counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54; the adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(15) Regarding claim 17:

Fujii discloses wherein utilizing the combinatorial logic includes generating a new rotate down signal based on an underflow in the adder (for the counter 4, if the count value becomes +M (overflow), the counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54; the adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(16) Regarding claim 19:

Fujii discloses a circuit comprising:

a controller (phase frequency detector (pfd) 2 in figure 2) for generating first rotate up and first rotate down signals (LEAD or LAG signal from PFD 2 in figure 2) for phase adjusts in a receiver link to adapt to frequency offsets (phase frequency detector 2 for comparing the output of the oscillating circuit 7 and a signal IN given to an input terminal 1 to emit a signal LEAD or LAG according to the phase difference, column 3, line68 – column 4, line 3); and

an adjust circuit (random walk filter (RWF) 3 and up down counter 4 in figure 2) coupled to the controller (RWF 3 is connected to the PFD 2 as shown in figure 2), the adjust circuit for detecting trends in the signals (the internal up and down counter of the RWF 3 accumulate the LEAD , LAG signal from the PFD 2 and the counter 4 output a adjust signal to the adder 6 according to the accumulation of the LEAD and LAG signal from the PFD 2, column 3, liens 68 – column 4, line 16) , and using combinatorial logic (adder 6 in figure 2) to adapt the signals based on accumulated data by generating second rotate up and second rotate down signals (adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62) improving a rate of compensation for the frequency offsets by the phase adjusts (the present invention object is to provide a phase locked loop in which the freedom of choice of the loop bandwidth is large and therefore a desire loop bandwidth can be obtained, column 6, lines 21-23; it is well known in the art that for a phase lock loop with a desire loop bandwidth will improve the system response and thus improve rate of compensation for the frequency offset), and wherein the adjust circuit monitors for an overflow of the first rotate up and rotate down signals (counter 4 with respect to figure 5, if the UP is entered from the random walk filter 3, the internal up-down counter operates by +1, if the DOWN is entered, then by -1, the UP and DOWN are sequentially calculated to accumulate the result; if the count value becomes +M (overflow), even if the UP is further entered, the count value is not changed; if the count value becomes –M (underflow), even if the DOWN is further entered, the count value is not changed any

more; counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54).

(17) Regarding claim 20:

Fujii discloses wherein the adjust circuit monitors for an overflow by counting and accumulating the first rotate up and rotate down signals (counter 4 with respect to figure 5, if the UP is entered from the random walk filter 3, the internal up-down counter operates by +1, if the DOWN is entered, then by -1, the UP and DOWN are sequentially calculated to accumulate the result; if the count value becomes +M (overflow), counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54).

(18) Regarding claim 21:

Fujii discloses wherein the adjust circuit monitors for an overflow with an up/down counter coupled to an adder (counter 4 with respect to figure 5, if the UP is entered from the random walk filter 3, the internal up-down counter operates by +1, if the DOWN is entered, then by -1, the UP and DOWN are sequentially calculated to accumulate the result; if the count value becomes +M (overflow), counter 4 emits this count value to the adder 6 as the n-bit signal, column 4, lines 45-54).

(19) Regarding claim 22:

Fujii discloses wherein the adjust circuit generates the second rotate up and rotate down signals through detection of overflow and underflow in the adder (counter 4, with respect to figure 5, if the UP is entered from the random walk filter 3, the internal up-down counter operates by +1, if the DOWN is entered, then by -1, the UP and DOWN are sequentially calculated to accumulate the result; if the count value becomes

+M (overflow), counter 4 emits this count value to the adder 6 as the n-bit signal and reset to zero; if the count value becomes –M (underflow), counter 4 emits this count value to the adder 6 as the n-bit signal and reset to zero, column 4, lines 45-54) and logically combines by the combinatorial logic the overflow and underflow with the first rotate up and rotate down signals (the adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62).

(20) Regarding claim 23:

Fujii discloses wherein the rotate up and rotate down signals are first rotate up and rotate down signals for phase adjusts in a receiver link to adapt to frequency offsets and causing rotation of a phase of a clock signal up or down to compensate for the frequency offsets (phase frequency detector 2 for comparing the output of the oscillating circuit 7 and a signal IN given to an input terminal 1 to emit a signal LEAD or LAG according to the phase difference, column 3, line68 – column 4, line 3, the LEAD LAG signal is connected to the adder 6 for generating adjusting signal to the oscillator 7), and wherein the combinatorial logic outputs second rotate up and rotate down signals (adder 6 adds the output of the counter 4 and the output of the register 5 to emit the result to the oscillator 7, column 4, lines 60-62) which improve a rate of compensation for the frequency offsets by the phase adjusts, the improvement relative to the compensation provided by using only the first rotate up and rotate down signals for adapting to the frequency offsets (the present invention object is to provide a phase locked loop in which the freedom of choice of the loop bandwidth is large and therefore a desire loop bandwidth can be obtained, column 6, lines 21-23; it is well known in the

art that for a phase lock loop with a desire loop bandwidth will improve the system response and thus improve rate of compensation for the frequency offset).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii (US 5,349,309).

(1) Regarding claim 12 (the examiner interprets the claim as the adder accumulating the chosen most significant of the up/down counter as disclose in the application):

Fujii does not explicitly discloses the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals.

However, Fujii discloses in column 4, lines 27-40 that the RWF 3 reads the output of the phase/frequency detector 2 at a predetermined clock cycle. If the input at that time is LEAD, then the internal up-down counter operates by +1, if LAG, then by -1 and if neither of them, then by 0 respectively; if the count value of the up-down counter adds up to +N, then the UP is emitted to return to the initial value (0). On the other hand, if the count value of the up-down counter becomes -N, then the DOWN is emitted to return to the initial value.

The up and down signal from the RWF 3 will cause the counter 4 to increase by 1 or decrease by 1. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to interpret the up and down signal from the RWF 3 to be the most significant bit of the internal counter of the RWF 3. As the internal counter of RWF 3 reaches N, the RWF will send a up signal to the counter 4 to increase the count value of the counter 4 by 1, and when the counter value reaches –N, the RWF 3 will sent a down signal to the counter 4 to decrease the count value of the counter 4 by 1.

The examiner interprets than when the count value of the internal up down counter of RWF 3 reaches N, the most significant bit of the counter will be the up signal that causes the counter 4 to increase by 1 and when the count value of the internal up down counter of RWF 3 reaches –N, the most significant bit of the counter will be the down signal to cause the counter 4 to reduce by 1.

(2) Regarding claim 18:

Fujii discloses wherein the phase adjusts further comprise rotate up and rotate down signals for phase rotation in the clock-data-recovery circuit (the RWF 3 output up and down signal to the counter 4 as shown in figure 2).

Fujii does not explicitly discloses the adder accumulates a chosen number of most significant bits of the rotate up and rotate down signals.

However, Fujii discloses in column 4, lines 27-40 that the RWF 3 reads the output of the phase/frequency detector 2 at a predetermined clock cycle. If the input at that time is LEAD, then the internal up-down counter operates by +1, if LAG, then by -1 and if neither of them, then by 0 respectively; if the count value of the up-down counter

adds up to +N, then the UP is emitted to return to the initial value (0). On the other hand, if the count value of the up-down counter becomes -N, then the DOWN is emitted to return to the initial value.

The up and down signal from the RWF 3 will cause the counter 4 to increase by 1 or decrease by 1. Therefore, it would have been obvious to interpret the up and down signal from the RWF 3 as the most significant bit of the internal counter of the RWF 3. As the internal counter of RWF 3 reaches N, the RWF will send a up signal to the counter 4 to increase the count value of the counter 4 by 1, and when the counter value reaches –N, the RWF 3 will sent a down signal to the counter 4 to decrease the count value of the counter 4 by 1.

The examiner interprets than when the count value of the internal up down counter of RWF 3 reaches N, the most significant bit of the counter will be the up signal that causes the counter 4 to increase by 1 and when the count value of the internal up down counter of RWF 3 reaches –N, the most significant bit of the counter will be the down signal to cause the counter 4 to reduce by 1.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Makarov (US 7,075,948 B2) discloses a frequency offset estimator. Usui (US 6,269,128 B1) discloses a clock recovery control in differential detection. Cranford, Jr. et al. (US 2002/0146084 A1) discloses an apparatus and method for oversampling with evenly spaced samples.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Siu M Lee/
Examiner, Art Unit 2611
4/5/2008

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611